

REMARKS

This present amendment is in response to the Final Office Action mailed December 3, 2002, and the correspondence from Examiner. Claims 1 and 9 have been amended. Applicants have thoroughly reviewed the outstanding Office Action including the Examiner's remarks and the references cited therein. The following remarks are believed to be fully responsive to the Final Office Action and, when coupled with the above amendments, are believed to render all claims at issue patentably distinguishable over the cited references.

Applicants respectfully request reconsideration in light of the above amendments and the following remarks.

Response to Correspondence

With respect to the Final Office Action, and the correspondence from the Examiner, the Examiner is of the opinion that the prior art of record all teach the method of forming a MOSFET as clearly outlined in the Final Rejection.

Applicant respectfully traverses these rejections.

The Amended Claimed invention recites that the MOSFET is formed by forming a gate and spacer in a trench to reduce the junction depth of the source/drain region. Gardner discloses that **spacer 32 has to first be formed on the sidewall of the trench 20** and the nitride layer 16, as shown in FIG. 5, and the **gate conductor 40 is then formed between spacers 32**, as shown in FIG. 7 (col. 7, line 43-46). “**The gate 40 of Gardner et al will be filled in the**

entire trench 20 if there is no sidewall 32 that is formed prior to the gate." The device will fail. Thus, the steps cannot be changed. On the contrary, in the Amended Claimed invention, the gate conductor is defined and first formed in the trench, and the spacers are then formed on the sidewall of the trench and the gate conductor, but the spacers **ARE NOT** formed on the nitride layers as taught in Gardner because the nitride layers are **NOT NECESSARY** for this invention.

Secondly, in Gardner, the LDD region 42 is first formed in the substrate 10 located at the bottom of the trench 20, and the S/D regions 50 are then formed in the substrate 10 beside the trench 20, wherein the spacers have to be pre-removed before forming the S/D regions 50, otherwise the LDD regions 42 and the S/D regions 50 would not be formed. It is to be noted that the spacers 32 have to be removed before forming the S/D regions. It is impossible to form the S/D regions without removing the spacers since the layer 16 and the spacer 32 will block ion penetration. However, the S/D regions of the Amended Claimed invention are directly formed without removing the sidewall spacer. The **nitride layers 16 must exist for Gardner because the layer 16 is used as an ion-barrier layer during formation of the LDD regions 42, so the formation of the nitride layer 16 and the process for removing the spacer 32** are critical for Gardner et al. Thus, the amended claimed invention is non-obvious over Gardner et al in view of either Hus et al or Brigham et al.

As mentioned, two ion-implanting processes and two processes for removing dielectric layer must be performed in Gardner et al for forming the S/D regions. On the contrary, the nitride layer is **unnecessary** in the Amended Claimed invention, because the formation of the ion-implanting region does not utilize the ion-barrier

layer, so there is no dielectric layer formed besides the trench structure before forming the S/D regions. Therefore, in the amended claimed invention, the S/D regions and the extended regions thereof can be formed by a one time- ion-implanting process and a one time thermal process, especially the extended regions used to substitute for the LDD region formed by conventional methods. However, the amended claimed invention needn't perform the process for removing the dielectric layer in the formation of the ion-implanted region, and **"it only need perform the ion- implanting process one time."**

Accordingly, it is respectfully submitted that independent Claims 1 and 9 as currently presented are patentable over the cited art.

Conclusion

In light of the above amendments and remarks, Applicants respectfully submit that all pending Claims 1 through 18 as currently presented are in condition for allowance. Applicant has thoroughly reviewed that art cited but relied upon by the Examiner. Applicant has concluded that these references do not affect the patentability of these claims as currently presented. Accordingly, reconsideration is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in

fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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VERSION WITH MARKING TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1 and 9 are amended as follows:

1. A method for forming a MOSFET, said method comprises:
providing a wafer, wherein said wafer comprises a substrate;
forming a trench in said substrate;
forming a gate on a bottom of said trench;
forming a spacer on both sides of said gate and filling of said trench;
implanting an ion into said substrate which is on both sides of said spacer;
proceeding a first rapid thermal process to form a source/drain region and source/drain extend region in said substrate;
forming a metal layer on said gate, said spacer, and said source/drain region;
proceeding a second rapid thermal process to said metal layer to form a silicide layer on said gate and said source/drain region; and
removing [said] an unreacted and a remaining metal layer to remain said silicide layer on the top of said gate and on said source/drain region.

9. A method for forming a MOSFET, said method comprises:
providing a wafer, wherein said wafer comprises a substrate;
forming a trench in said substrate;
forming a gate on a bottom of said trench, wherein said gate comprises a gate oxide layer;

forming a spacer on a sidewall of said gate and said gate oxide layer and filling of said trench;

implanting [a] an ion into said substrate which is on both sides of said spacer;

proceeding a first rapid thermal process to form a source/drain region and a source/drain extend region in said substrate;

proceeding a second rapid thermal process to said metal layer to form a silicide layer on said gate and said source/drain region; [and]

removing [said] an unreacted and a remaining metal layer; and
proceeding a third rapid thermal process to said silicide layer.